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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/071,453	02/08/2002	Luan C. Tran	MI22-1921	1088

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EXAMINER
SCHILLINGER, LAURA M

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 04/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/071,453	TRAN, LUAN C.	
	Examiner	Art Unit	
	Laura M Schillinger	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *34-40 and 44-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *34-40 and 44-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *12* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in Response to Applicant's Communication filed on 3/6/03 in Paper No. 13.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 34-37 and 44-46 are rejected under 35 U.S.C. 102(e) as being anticipated by Liaw et al ('276).

In reference to claim 34, Liaw et al ('276) teaches a transistor assembly comprising:

A plurality of active areas having widths defined by STI (Fig.2 (14)) of no greater than one micron, at least some of the widths being different (Fig.2 (14)) (See also Abs., lines: 1-20); and

Gate lines disposed over the plurality of active areas to provide individual transistors, those transistors whose widths are different having different threshold voltages from one another (Fig.s 1 and 2 (13 NMOS and PMOS – see also Fig.4 showing the correlation between channel width and variation in threshold voltage (hereinafter referred to as T_v see also Col.4, lines: 10-25- Table).

In reference to claim 35, Liaw et al ('276) teaches wherein the T_v of at least some transistors are less than one volt (Fig.4 see also Col.4, lines: 10-25- Table).

In reference to claim 36, Liaw et al ('276) teaches wherein individual transistors having active areas with smaller widths have T_v which are smaller than other individual transistors having active areas with larger widths (Fig.4 see also Col.4, lines: 10-25- Table)

In reference to claim 44, Liaw et al ('276) teaches a transistor assembly comprising:

An active area (Fig.2 (12));

A plurality of spaced-apart STI regions received by the active area and defining active sub-areas there between, individual active sub-areas having respective widths, at least one of the widths being no greater than about one micron and at least one other sub-area having a width which is different from the one width (Fig.2 (14) and Abs., lines: 1-20); and

A gate line extending over the one and other sub-area and defining in part, separate transistors, wherein each of the separate transistors has a different T_v (Figs.1 and 2 (13 and 15 NMOS and PMOS, see Figure 4 and see also Col.4, lines: 10-25- Table).

In reference to claim 45, Liaw et al ('276) teaches wherein each active sub-area width of an associated transistor is no greater than about one micron (Abs., lines: 1-20).

In reference to claim 46, Liaw et al ('276) teaches wherein each active sub-area width of an associated transistor is no greater than about one micron, wherein more than two separate transistors have different T_v (Figure 4 and see also Col.4, lines: 10-25- Table).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 37, 39-40 and 47-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liaw et al ('276) as applied to claim 34 above, and further in view of Sunouchi et al ('422).

In reference to claims 37, 39-40 and 47-48 Liaw teaches a gate line having a plurality of active sub-areas defining a plurality of transistors, each active area sub-area width of an associated transistor being no greater than about one micron (Abs., lines: 1-20 and Fig.2 NMOS/ PMOS).

In reference to claim 49-50, Liaw et al ('276) teaches a transistor assembly comprising:

An active area (Fig.2 (12));

A plurality of spaced-apart STI regions received by the active area and defining active sub-areas there between, individual active sub-areas having respective widths, at least one of the widths being no greater than about one micron and at least one other sub-area having a width which is different from the one width (Fig.2 (14) and Abs., lines: 1-20); and

A gate line extending over the one and other sub-area and defining in part, separate transistors, wherein each of the separate transistors has a different T_v (Figs.1 and 2 (13 and 15 NMOS and PMOS, see Figure 4 and see also Col.4, lines: 10-25- Table) active sub-area width of an associated transistor is no greater than about one micron (Figure 4 and see also Col.4, lines: 10-25- Table)..

However fails to teach further comprising a common gate line, which extends over the active area transistors (in parallel configuration) for a DRAM or DRAM circuitry. However, Sunouchi teaches implementing MOS transistors for DRAM circuitry and includes a common gate line formed over parallel transistors having active areas with different widths (Fig.34 (WL)- See also Fig.37(A- STIs 32)). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Liaw's teachings to include a common gate and transistors in parallel configuration because as Sunouchi teaches, common gate lines are used to provide interconnection to transistors implemented within DRAM circuitry (Col.1, lines: 20-25 and Col.4, lines: 55-65, see also Col.10, lines: 10-15).

Claims 38 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liaw et al ('276) as applied to claim 34 above, and further in view of Sunouchi et al ('422) and Lu et al ('134).

In reference to claims 38 and 39, Liaw teaches the limitations of the MOS transistor as claimed by the applicant, Sunouchi teaches implementing a similar MOS to make up DRAM circuitry however fails to give specifics of the circuitry to include wherein one transistor comprises a pass transistor nor wherein one of the individual transistors comprises a portion of sense amplifier circuitry for a DRAM and has a lower T_v. However, Lu teaches implementing MOS transistors (having STI) in DRAM circuitry wherein one MOS is a pass transistor and another set of MOS transistors is implemented in a sense amplifier for the DRAM (Col.Col.4, lines: 15-45). It would have been obvious to one of ordinary skill in the art to combine the MOS taught by Liaw to be implemented within the DRAM circuitry taught by Sunouchi because Sunouchi teaches the implementation of varied width channel transistors having minimum element isolation width F within a DRAM (Abs., lines: 1-10), further it would have been obvious to include the pass transistor and sense amplifier circuitry taught by Lu within Sunouchi's DRAM circuitry since Lu teaches such circuitry is peripheral circuitry which is typically found within DRAM devices and is further dependent upon T_v (Col.1, lines: 15- 45).

Response to Arguments

Applicant requested that the claims be readdressed with the proper numbering- the Examiner has complied.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura M Schillinger whose telephone number is (703) 308-6425. The examiner can normally be reached on M-T, R-F 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W Whitehead, Jr. can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

LMS
April 4, 2003